wherein the monocrystalline compound semiconductor material is piezoelectric, and wherein the monocrystalline compound semiconductor material thickness is between about 0.5 μm and 10 μm.

56. The semiconductor structure of claim 55 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

57. The semiconductor structure of claim 55 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

58. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material; and

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material, wherein the monocrystalline compound semiconductor material is piezoelectric, and

wherein the monocrystalline compound semiconductor material creates a reflective surface.

59. The semiconductor structure of claim 58 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

60. The semiconductor structure of claim 58 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

61. The semiconductor structure of claim 58 wherein the monocrystalline compound semiconductor material thickness is between about 0.05 μm and 100 μm.

62. The semiconductor structure of claim 58 further comprising an integrally formed electrical component in communication with the reflective surface of the monocrystalline compound semiconductor material.

63. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material; and

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material, wherein the monocrystalline compound semiconductor material is piezoelectric,

further comprising a reflective material overlying the monocrystalline compound semiconductor material.

64. The semiconductor structure of claim 63 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

65. The semiconductor structure of claim 63 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

66. The semiconductor structure of claim 63 wherein the monocrystalline compound semiconductor material thickness is between about 0.05 μm and 100 μm.

67. The semiconductor structure of claim 63 further comprising an integrally formed electrical component in communication with the reflective material overlying the monocrystalline compound semiconductor material.

68. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material; and

a piezoelectric material overlying the monocrystalline compound semiconductor material

wherein the piezoelectric material is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material,

wherein the piezoelectric monocrystalline semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide, and

wherein the piezoelectric monocrystalline semiconductor material thickness is between about 0.05 μm and 10 μm.

69. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material; and

a piezoelectric material overlying the monocrystalline compound semiconductor material

wherein the piezoelectric material is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material,

wherein the piezoelectric monocrystalline ceramic material is selected from the group consisting of barium titanate, lead titanate, potassium niobate, lead niobate, and lead zirconate titanate, and

wherein the piezoelectric monocrystalline semiconductor material thickness is between about 0.5 μm and 200 μm.

70. The semiconductor structure of claim 69 wherein the piezoelectric ceramic material thickness is between about 5 μm and 25 μm.

71. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material; and

a piezoelectric material overlying the monocrystalline compound semiconductor material

wherein the piezoelectric material creates a reflective surface.

72. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material; and

a piezoelectric material overlying the monocrystalline compound semiconductor material,

further comprising a reflective material overlying the piezoelectric material.

73. The semiconductor structure of claim 71 further comprising an integrally formed electrical component in communication with the reflective surface of the piezoelectric material.

74. The semiconductor structure of claim 72 further comprising an integrally formed electrical component in communication with the reflective material overlying the piezoelectric material.

75. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film, wherein the monocrystalline compound semiconductor layer is piezoelectric,

wherein the monocrystalline compound semiconductor layer is formed to a thickness between about 0.5 μm and 10 μm.

76. The process of claim 75 further comprising depositing at least one conductive element in contact with the monocrystalline compound semiconductor layer.

77. The process of claim 75 wherein the material to epitaxially form the monocrystalline compound semiconductor layer is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

78. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film, wherein the monocrystalline compound semiconductor layer is piezoelectric,

wherein the monocrystalline compound semiconductor layer is formed with a reflective surface.

79. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film, wherein the monocrystalline compound semiconductor layer is piezoelectric

further comprising adhering a reflective material to the monocrystalline compound semiconductor layer.

80. The process of claim 78 further comprising integrating an electrical component with the monocrystalline compound semiconductor layer wherein the electrical component is in communication with the reflective surface.

81. The process of claim 79 further comprising integrating an electrical component with the monocrystalline compound semiconductor layer wherein the electrical component is in communication with the reflective material.

82. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer,

wherein the material to form the piezoelectric material layer is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material, and

wherein the piezoelectric monocrystalline ceramic material is selected from the group consisting of barium titanate, lead titanate, potassium niobate, lead niobate, and lead zirconate titanate.

83. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer,

wherein the material to form the piezoelectric material layer is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material, and

wherein the piezoelectric monocrystalline semiconductor material is formed to a thickness between about 0.05 μm and 100 μm.

84. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer,

wherein the material to form the piezoelectric material layer is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material, and

wherein the piezoelectric semiconductor material is formed to a thickness between about 0.5 μm and 10 μm.

85. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer,

wherein the material to form the piezoelectric material layer is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material and

wherein the piezoelectric monocrystalline ceramic material is formed to a thickness between about 0.5 μm and 200 μm.

86. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer,

wherein the material to form the piezoelectric material layer is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material, and

wherein the piezoelectric ceramic material is formed to a thickness between about 5 μm and 25 μm.

87. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer

wherein the piezoelectric material layer is formed with a reflective surface.

88. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer

further comprising adhering a reflective material to the piezoelectric material layer.

89. The process of claim 87 further comprising integrating an electrical component with the piezoelectric material layer wherein the electrical component is in communication with the reflective surface.

90. The process of claim 88 further comprising integrating an electrical component with the monocrystalline compound semiconductor material wherein the electrical component is in communication with the overlying reflective material.--

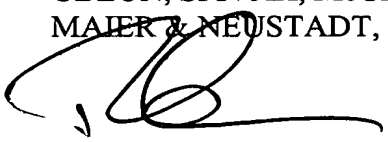
SUPPORT FOR AMENDMENT

The above new claims place those claims indicated as being allowable in

proper form, and thus place this case in condition for allowance. Early notification to this effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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IN THE CLAIMS

Claims 1-54 (Canceled)

Claims 55-90 (New)

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